PTO
10/055568
01/22/02

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10055568	01/22/2002	~~257~~ 257		2841	

**APPLICANTS: Lin Mou-Shiung; Lee Jin-Yuan; Huang Ching-Cheng;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
TAIWAN 90133195 12/31/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		
Verified and Acknowledged Examiner's Initials			JCLA 9533

TITLE : Integrated chip package structure using silicon substrate and method of manufacturing the same

U.S. DEPT. OF COMM. PAT. & TM. FORM-436/Rev. 12-81

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

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